REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-16 are pending in the present application. Claims 1, 2, 4-10, 13, and 14 are amended by the present amendment.

In the outstanding Office Action, Claims 1-16 were objected to; Claims 4-9 were rejected under 35 U.S.C. § 112, second paragraph; Claims 1 and 10 were rejected under 35 U.S.C. § 102(b) as anticipated by Igarashi (U.S. Patent No. 6,057,728); Claims 1, 10-13, 15, and 16 were rejected under 35 U.S.C. § 102(b) as anticipated by Takizawa et al. (U.S. Patent No. 5,926,012, herein "Takizawa"); and Claims 1-9 and 14 were indicated as allowable if rewritten in independent form.[1]

Applicants thank the examiner for the indication of allowable subject matter and for the courtesy of an interview extended to Applicants' representative on November 2, 2005. During the interview, the differences between the claims and the applied art were discussed. Further, clarifying claim amendments, similar to those presented herewith, were also discussed. The examiner indicated he would further review the amended claims in view of a filed response. Arguments presented during the interview are reiterated below.

In view of the indication of allowable subject matter in Claims 2, 3, and 14, Claims 2 and 14 have been rewritten in independent form to include all the features of their base claims. No new matter has been added. Thus, it is believed that Claims 2-9 and 14 are in condition for allowance.

[1] It is noted that the outstanding Office Action indicates at page 6, numbered paragraph 7, that Claims 1-9 and 14 includes allowable subject matter. However, it is believed that the outstanding Office Action incorrectly lists Claims 1-9 and 14.

Regarding the objection to Claims 1-16, Claims 1, 2, 6, 7, 10, 13, and 14 have been amended as suggested in the outstanding Office Action without adding new matter. Accordingly, it is respectfully requested this objection be withdrawn.

Regarding the rejection of Claims 4-9 under 35 U.S.C. § 112, second paragraph, Claims 4-9 have been amended as suggested in the outstanding Office Action without adding new matter. Accordingly, it is respectfully requested this rejection be withdrawn.

Regarding the rejection of Claims 1 and 10 under 35 U.S.C. § 102(b) as anticipated by Igarashi, independent Claim 1 has been amended to recite that a driver "includes first and second drive circuits" and each drive circuit is controlled by a timing controller through a corresponding electrical connection, Claim 10 has been amended to recite the "driver including first, second, and third drive circuits," and both Claims 1 and 10 have been amended to correct minor informalities. The claim amendments find support in Figures 1, 4, and 7 and in their corresponding description in the specification. No new matter has been added.

Briefly recapitulating, amended Claim 1 is directed to a drive circuit that includes a driver that applies a gate voltage to a transistor, and a timing controller that controls a timing of the driver. The driver includes first and second drive circuits, the first and second drive circuits are electrically connected to the timing controller through first and second electrical connections, respectively, and the first and second electrical connections control the first and second drive circuits, respectively. The driver is capable of applying the gate voltage as a first gate voltage through the first drive circuit to the transistor, and as a second gate voltage through the second drive circuit to the transistor.

In a non-limiting example, Figure 1 shows the driver 2, the first drive circuit 22, the second drive circuit 21, the timing controller 3, the first electrical connection (connection

between elements 34 and 22), and the second electrical connection (connection between elements 33 and 21).

Turning to the applied art, Igarashi shows in Figure 2 a driver 20 having a timing controller 7a and 7b, and a buffer circuit that includes NPN transistor 7c and PNP transistor 7d. The transistors 7c and 7d are connected between an undisclosed voltage and ground. The outstanding Office Action asserts at page 4, numbered paragraph 5, that transistors 7c and 7d are capable of applying a first gate voltage and a second gate voltage to a transistor 1. However, as discussed during the interview, first and second transistors 7c and 7d in Igarashi are not connected through first and second electrical connections to the timing controller 7a and 7b. Therefore, Igarashi does not teach or suggest first and second electrical connections that control first and second drive circuits, respectively, as required by amended Claim 1.

Accordingly, it is respectfully submitted that independent Claim 1 and each of the claims depending therefrom patentably distinguish over Igarashi.

Regarding independent Claim 10, Claim 10 recites a voltage supply unit that generates a gate voltage that is applied to a transistor based on a main current of the transistor, and a driver that applies the gate voltage to the transistor. The driver includes first, second, and third drive circuits, the first and second drive circuits apply first and second gate voltages to the transistor, and the third drive circuit applies the gate voltage.

In a non-limiting example, Figure 7 shows the voltage supply unit 5 that applies a voltage Vc based on a main current (signal from block 1 entering block 6) of the transistor 1. In addition, as shown in Figure 4, the driver 2 includes first drive circuit 25, second drive circuit 23, and third drive circuit 24.

However, as discussed during the interview, Igarashi does not teach or suggest (i) a third drive circuit, and (ii) a gate voltage applied by the third drive circuit being determined based on a main current of the transistor, as required by amended Claim 10.

Accordingly, it is respectfully submitted that independent Claim 10 and each of the claims depending therefrom patentably distinguish over Igarashi.

Regarding the rejection of Claims 1, 10-13, 15, and 16 under 35 U.S.C. § 102(b) as anticipated by Takizawa, that rejection is respectfully traversed for the following reasons.

Takizawa shows in Figure 15 an arrangement similar to the arrangement of Igarashi, i.e., a driver including two transistors (not labeled) coupled between the power sources 36 and 37 and a controlling transistor 33 coupled to a switch transistor 1. However, as discussed during the interview regarding Claim 1, Takizawa does not teach or suggest a timing controller controlling first and second drivers through first and second electrical connections, respectively. On the contrary, Takizawa shows in Figure 15 that both transistors are controlled by a ***single*** electrical connection.

Regarding Claim 10, it is noted that even if transistor 33 shown in Figure 15 of Takizawa is asserted to correspond to the claimed third drive circuit, transistor 33 applies the voltage provided by source 36, which is not different from the voltage applied by the upper transistor of the driver. In other words, Takizawa does not teach or suggest applying a gate voltage and first and second gate voltages such that the gate voltage is different from the first and second gate voltages.

Accordingly, it is respectfully submitted that independent Claims 1 and 10 and each of the claims depending therefrom patentably distinguish over Takizawa.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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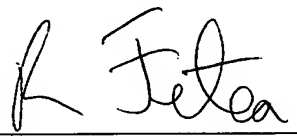

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